All corrections are approved. 8/14/06 JPL

In The Specification:

In accordance with Rule § 1.121 , please amend the specification by substituting the following replacement paragraphs. All deleted material is shown by strike-through effects. All added text is underlined. No new matter is added by the amendments listed below:

Page 1, lines 18-24:

For example, in the case of the X16 memory device with four banks, four I/O pins are used ~~correspondent~~ corresponding to the four banks and 16 I/O lines are compressed into one I/O line internal memory chip. Consequently, 16 I/O pins are compared simultaneously. In the same way, all memory cells of the four banks can be simultaneously tested [[only]] with only four pins if one pin is assigned to each bank.

Page 2, lines 8-16:

The conventional I/O compression test circuit comprises four test blocks 1~4, a fail detection block 5, and a strobe block 6. 16 I/O global lines GIO<0:15> are divided into four groups, which are tested by the test blocks 1~4. The fail detection block 5 compares test results of the test blocks 1~4 to detect a failure. The strobe block 6 outputs an output signal [[from]] to the fail detection block 5 synchronously with respect to a strobe signal STN.

Page 4, lines 7-10:

If one of the output signals TBS1~TBS4 from the test blocks 1~4 becomes at a low level, that is, a [[fail]] failure occurs, an output signal from the NAND gate ND1 becomes at a high level.

Page 5, lines 1-4:

representing a test mode. The delay block 8 delays an output signal from the NAND gate ND5 for a predetermined time. Here, the delay block 8 comprises [[the]] an even number of inverters.

Page 5, lines 11-13:

Fig. 2 is a circuit diagram illustrating an example of the test block 1 of Fig. 1. ~~The rest test~~ Test blocks 2~4 have the same structure as that of the test block 1.

Page 9, lines 4-7:

Fig. 3 is a block diagram of an I/O compression test circuit according to an embodiment of the present invention. The I/O compression test circuit [[test]] tests 16 global I/O lines GIO<0:15> at the same time.

Page 9, lines 20-22:

Fig. 4 is a circuit diagram of the test block 10 of Fig. 3. ~~The rest test~~ Test blocks 20, 30, and 40 have the same structure as that of the test block 10.

Page 12, lines 3-21:

The control block 50 comprises NAND gates ND12~ND14, an inverter [[12]] INV12, a first delay block 51 and a second delay block 52. The NAND gate ND12 performs an NAND operation on a signal GIOSTP representing when data are transmitted into the global I/O lines GIO and a signal TMCOMP representing a test mode. The first delay block 51 delays an output signal from the NAND gate ND12 for a predetermined time. The NAND gate ND13 performs an NAND operation on output signals from the NAND gate ND12 and the first delay block 51. The inverter INV12 inverts an output signal from the NAND gate ND13 to output a strobe signal SACLK. The second delay block 52 delays the strobe signal SACLK outputted from the inverter for a predetermined time to output a delay strobe signal SACLKD. The NAND gate ND14 performs an

NAND operation on the signal TMCOMP representing a test mode and the output signal from the NAND gate ND12, and outputs a reset signal RESET. Here, each delay block 51 and 52 comprises an inverter chain including [[the]] an odd number of inverters.

Page 13, lines 2-7:

The ~~output signal from the NAND gate ND12 is delayed by the first delay block 51, and the~~ strobe signal SACLK as a pulse signal is outputted through the first delay block 51, the NAND gate ND13, and the inverter INV12. The strobe signal SACLK controls test timing of the test blocks 10, 20, 30 and 40.

Page 14, lines 15-18:

[[IF]]If the reset signal RESET is enabled to a high level, the NMOS transistor NM19 and the PMOS transistor PM19 precharge the input terminals UP and DN to the ground voltage and the power voltage, respectively.